

## WEST Search History

[Hide Items](#)[Restore](#)[Clear](#)[Cancel](#)

DATE: Tuesday, January 06, 2004

<b>Hide?</b>	<b><u>Set Name</u></b>	<b><u>Query</u></b>	<b><u>Hit Count</u></b>
	<i>DB=USPT; PLUR=YES; OP=ADJ</i>		
<input type="checkbox"/>	L15	(synchronous coherent)	62
<input type="checkbox"/>	L12	L11 not l10	14
<input type="checkbox"/>	L11	L8.ab.	15
<input type="checkbox"/>	L10	L8.ti.	3
<input type="checkbox"/>	L9	L8.ti,ab.	17
<input type="checkbox"/>	L8	L7 near15 (dma or direct memory access)	391
<input type="checkbox"/>	L7	(shared or global) near3 (memory or ram)	13563
<input type="checkbox"/>	L6	L3.ti,ab.	3
<input type="checkbox"/>	L5	L3 and (dma or direct memory access)	3
<input type="checkbox"/>	L3	(memory or ram) near3 (non\$1adjacent or ("not" adj adjacent))	48
<input type="checkbox"/>	L2	('4486834' '5568609')[URPN]	12
<input type="checkbox"/>	L1	(4486834 or 5568609).pn.	2

END OF SEARCH HISTORY

First Hit   Fwd Refs



Generate Collection

L2: Entry 7 of 12

File: USPT

Aug 20, 1996

US-PAT-NO: 5548743

DOCUMENT-IDENTIFIER: US 5548743 A

**\*\* See image for Certificate of Correction \*\***

TITLE: Data processing system with duplex common memory having physical and logical path disconnection upon failure

First Hit    Fwd Refs

☐ Generate Collection

L10: Entry 1 of 3

File: USPT

Dec 10, 1996

DOCUMENT-IDENTIFIER: US 5584010 A

TITLE: Direct memory access control device and method in a multiprocessor system  
accessing local and shared memory

First Hit    Fwd Refs

☐ Generate Collection

L12: Entry 3 of 14

File: USPT

Sep 19, 2000

DOCUMENT-IDENTIFIER: US 6122699 A

**\*\* See image for Certificate of Correction \*\***

TITLE: Data processing apparatus with bus intervention means for controlling interconnection of plural busses

Abstract Text (1):

This invention has as its object to improve the net processing speed by appropriately assigning the DMA processing time for attaining high-speed processing using hardware, and the software execution time of a CPU. By interrupting the operation of one of a CPU and a DMA processor only when a device such as an external D-RAM shared by processors such as the CPU, DMA processor, and the like, is to be accessed, the CPU operation and the DMA processing are substantially parallelly executed, thereby improving the net processing speed.